WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device, comprising:

a first MISFET having a first gate insulating film formed over a first element forming region of a main surface of a semiconductor substrate and a first gate electrode formed over said first gate insulating film; and

a second MISFET having a second gate insulating film formed over a second element forming region of said main surface of said semiconductor substrate and a second gate electrode formed over said second gate insulating film,

said second gate insulating film being thinner than said first gate insulating film,

wherein said first gate insulating film includes a thermally oxidized film and a deposited film,

wherein said second gate insulating film includes a thermally oxidized film,

wherein said first element forming region and said second element forming region are individually isolated by an element isolation region, and

wherein said deposited film extends over said element isolation region such that an edge portion of said first gate electrode is formed over said deposited film at a portion of said deposited film positioned over said element isolation region.

2. A semiconductor integrated circuit device according to claim 1, wherein said element isolation region includes an isolating material buried in a groove formed in said substrate.

3. A semiconductor integrated circuit device according to claim 1, wherein said deposited film is formed by a vapor deposition method.

4. A semiconductor integrated circuit device according to claim 1, wherein said vapor deposition method is a chemical vapor deposition method.

5. A semiconductor integrated circuit device, comprising:

a first MISFET having a first gate insulating film formed over a semiconductor substrate and a first gate electrode formed over said first gate insulating film; and

a second MISFET having a second gate insulating film formed over said semiconductor substrate and a second gate electrode formed over said second gate insulating film,

said second gate insulating film of said second MISFET being thinner than said first gate insulating film,

wherein said first gate insulating film extends over an insulating film having a thickness greater than that of said first gate insulating film, and an edge portion of said first gate electrode in a gate width direction thereof is formed over a portion of said first gate insulating film positioned over said insulating film.

6. A semiconductor integrated circuit device according to claim 5, wherein said insulating film is buried in a groove formed in said substrate.

7. A semiconductor integrated circuit device according to claim 5, wherein said insulating film is integrally formed with an element isolation film defining a first MISFET forming region.

8. A semiconductor integrated circuit device according to claim 5, wherein said first gate insulating film includes a deposited film, and wherein said second gate insulating film includes a thermally oxidized film.

9. A semiconductor integrated circuit device according to claim 8, wherein said deposited film is formed by a vapor deposition method.

10. A semiconductor integrated circuit device according to claim 9, wherein said vapor deposition method is a chemical vapor deposition method.

11. A semiconductor integrated circuit device according to claim 5, wherein said first gate insulating film is formed by a vapor deposition method.

12. A semiconductor integrated circuit device according to claim 11, wherein said vapor deposition method is a chemical vapor deposition method.

13. A semiconductor integrated circuit device, comprising:

a first MISFET having a first gate insulating film formed over a semiconductor substrate and a first gate electrode formed over said first gate insulating film; and

a second MISFET having a second gate insulating film formed over said semiconductor substrate and a second gate electrode formed over said second gate insulating film,

said second gate insulating film of said second MISFET being thinner than said first gate insulating film,

wherein said first gate insulating film extends over an insulating film such that an edge portion of said first gate electrode is formed over said first gate insulating film at a portion of said first gate insulating film positioned over said insulating film,

wherein said insulating film is buried in a groove formed in said substrate, and

wherein said insulating film is integrally formed with an element isolation film defining a first MISFET forming region.

14. A semiconductor integrated circuit device according to claim 13, wherein said first gate insulating film includes a deposited film, and wherein said second gate insulating film includes a thermally oxidized film.

15. A semiconductor integrated circuit device according to claim 14, wherein said deposited film is formed by a vapor deposition method.

16. A semiconductor integrated circuit device according to claim 15, wherein said vapor deposition method is a chemical vapor deposition method.

17. A semiconductor integrated circuit device according to claim 13, wherein said first gate insulating film is formed by a vapor deposition method.

18. A semiconductor integrated circuit device according to claim 17, wherein said vapor deposition method is a chemical vapor deposition method.

19. A semiconductor integrated circuit device, comprising:

a first MISFET having a first gate insulating film formed over a semiconductor substrate and a first gate electrode formed over said first gate insulating film; and

a second MISFET having a second gate insulating film formed over said semiconductor substrate and a second gate electrode formed over said second gate insulating film,

said second gate insulating film of said second MISFET being thinner than said first gate insulating film,

wherein said first gate insulating film extends over an insulating film having a thickness greater than that of said first gate insulating film, and said first gate electrode is formed over said first gate insulating film including at a portion of said first gate insulating film positioned over said insulating film.

20. A semiconductor integrated circuit device according to claim 19, wherein said insulating film is integrally formed with an element isolation film defining a first MISFET forming region.

21. A semiconductor integrated circuit device according to claim 19, wherein said insulating film is buried in a groove formed in said substrate.

22. A semiconductor integrated circuit device according to claim 19, wherein said first insulating film is formed by a vapor deposition method.

23. A semiconductor integrated circuit device according to claim 22, wherein said vapor deposition method is a chemical vapor deposition method.

24. A semiconductor integrated circuit device according to claim 19, wherein said first gate insulating film includes a deposited film, and wherein said second gate insulating film includes a thermally oxidized film.

25. A semiconductor integrated circuit device according to claim 24, wherein said deposited film is formed by a vapor deposition method.

26. A semiconductor integrated circuit device according to claim 25, wherein said vapor deposition method is a chemical vapor deposition method.